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Soft-Switching Resonant Conversion with IGCT

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Abstract—In the area of medium voltage DC-DC conversion, series resonant converter is an attractive topology for implementation of the solid state DC transformer. Applying integrated gate controlled thyristor as a switch, it is possible to obtain very low conduction losses, while greatly lowering the switching losses by proper use of this converter topology. Continuous operation of the IGCT under low current turn-off and zero voltage turn-on is explored throughout this paper, with the emphasis of the proper dead-time selection, critical parameter limiting the increase of switching frequency while keeping the turn-off losses low. Theoretical assumptions and conclusions are supported by experimental results obtained from a dedicated test setup designed to emulate the operating conditions present in series resonant converter.

Index Terms—IGCT, Resonant Converters, High Power DC-DC, Solid State Transformers

I. INTRODUCTION

Motivation of exploring the Integrated Gate-Commutated Thyristor (IGCT) technology is found in extended research interests in Medium Voltage Direct Current (MVDC) power distribution networks with DC-DC converters taking a role of DC transformers. Marine sector has shown considerable interest lately for the introduction of DC distribution, as shown in [1] and [2], offering increased efficiency, lower count of the system components required for operation, and improved space utilization. Offshore wind farm energy collection based on MVDC grid with a variation of series resonant converter topology as a central system component is discussed in [3] and [4]. High Voltage Direct Current (HVDC) transmission has already been proven in the field as an alternative to the AC transmission for connecting off-shore generation to the on-shore loads or at very long distance interconnections. With a growing interest in HVDC, opportunity for direct MVDC or Low Voltage Direct Current (LVDC) transformation presents itself in order to distribute power to the various industrial or residential loads. One such converter, capable of interfacing HVDC to MVDC or LVDC is presented in [5].

Research done in [6] and [7] shows that much has already been done in the field, with a majority of solutions based on the Insulated Gate Bipolar Transistor (IGBT) technology. An alternative is found in the IGCT technology already present in medium voltage drives [8], rectifiers [9] variable speed drives, solid state breakers [10] etc. It is a mature technology with a typical application in circuits with hard-switching of the semiconductor device loaded with large currents and typical frequencies not higher than 900Hz. It is reported in [8] that the technology

have found its place in numerous pieces of equipment with over 1GW of installed power, even 20 years ago.

Advantages that IGCT clearly has over the IGBT are thoroughly presented in [11]. As a thyristor based device, conduction losses are greatly lower than of the IGBT of the same rating. Turn-on switching losses are usually negligible due to the clamping circuit required for hard-switching operation while the turn-off losses remain similar to the IGBT. High short-circuit capability and high reliability make IGCT ideal for high power applications. Smaller silicon surface for the same current rating together with an improved thermal contact with the package makes the IGCT a very compact solution. Possible drawback might be associated with the relatively large size of the gate driver unable to control the di/dt during the turn-on which further introduces a requirement for the clamp circuit.

Resonant converter topologies (e.g. [12]) present the opportunity to further maximize performance of the IGCT. Significant decrease in turn-off power losses could be achieved by low current turn-off. Low turn-on di/dt due to the load side resonant circuit challenges the idea of using the clamp circuit, lowering the element count in the final design.

This paper explores the quasi-soft switching of the IGCT under the typical LLC Series Resonant Converter (LLC-SRC) current and voltage stresses in continuous operation and show the increased switching frequency capability offered by the low current turn-off. Authors are not aware of any applications of the IGCT power switches in LLC-SRC or similar resonant topologies up to the moment of writing of this article. Thus, the paper provides, for the first time, insights into performances and capabilities of this kind of semiconductor devices, under somewhat unusual operating conditions.

II. CONTINUOUS MODE OF OPERATION

Typically, LLC-SRC converter topology works under the fixed duty cycle of 50% and controllable switching frequency for the output voltage regulation. Application of this topology in a solid state transformer, shows that a fixed switching frequency is preferred whereas load rejection within 5-10% limit can be achieved by proper tuning of the passive components' parameters with the resonant frequency slightly greater than the switching frequency. This kind of operation ensures nearly constant turn-off losses of the converter which are kept at minimum by proper selection of the turn-off current or further optimization of the switching element, IGCT in this case.

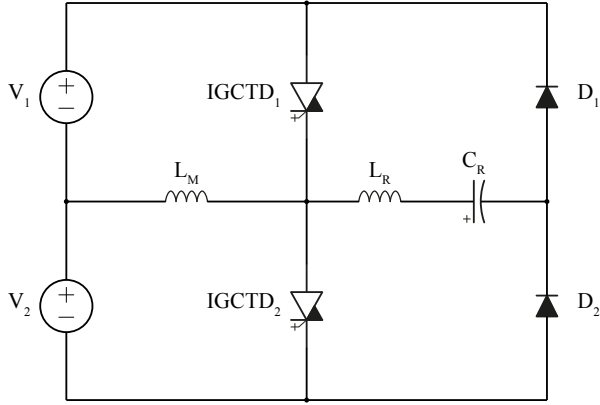


Figure 1: Equivalent circuit used for the theoretical analysis of the test setup

Simulation circuit representing the test setup is shown in the Fig. 1 and is a simplified version of the actual circuit. DC-link is split in half and connected to the reverse conducting IGCT (IGCT and an anti-parallel diode in the same package) half-bridge. Middle point of the DC-link is connected to one end of the magnetizing inductor L_M , while the other end of the inductor connects to the output of the half-bridge. By switching $IGCTD_1$ and $IGCTD_2$, half of the DC-link voltage is applied to the L_M in an alternating manner and the triangular current i_{Lm} is established (emulating the magnetizing current).

The other part of the circuit is responsible for the resonance. Resonant tank, consisting of the series connection of the L_R and C_R is connected to the output of the half-bridge on one end, and to the middle point of the diode half-bridge, $D_1 - D_2$, on the other. Diode half-bridge ensures the guidance of the resonant current through the proper IGCT for the LLC-SRC current stress emulation.

During the start-up of the test setup, resonant current i_{Lr} in the $L_R - C_R$ tank is started by first setting the proper initial voltage of the resonant capacitor C_R followed by triggering of the $IGCTD_2$. Since there are no losses in the simulation model, the resonance is supported on its own during the switching of the IGCT half-bridge. The simulation model is used to evaluate different working points of the test setup before running the actual tests. The results of one such simulation are given in Fig. 2 as an example to show the typical LLC-SRC current and voltage waveforms through the switching elements, achieved by the setup not requiring a full sized converter.

One of the essential requirements ensuring the safe and short-circuit resistant operation of the LLC-SRC bridge is proper definition of the required minimum dead-time - t_{Dmin} for the half-bridge branch i.e. time needed for the top IGCT to enter the blocking state before the bottom one is turned on. Parameter named turn-off delay time, t_{DOFF} is defined by the manufacturer as the time between the moment when control optical signal assumes value low (off command) and the moment when current through the IGCT falls to the 40% of the starting value [13]. This parameter is strongly influenced by the blocking voltage,

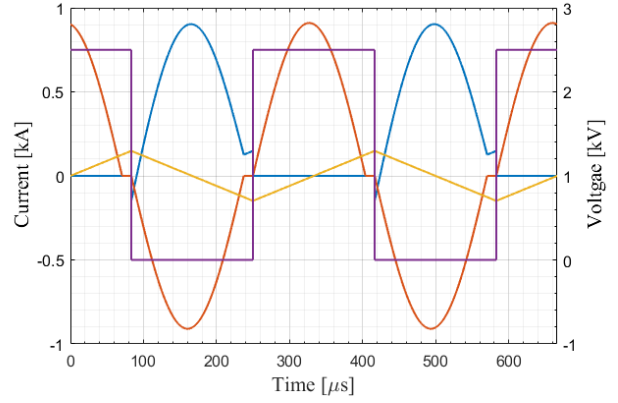


Figure 2: Typical waveforms for the circuit in Fig. 1; purple - $IGCTD_2$ voltage, blue - $IGCTD_2$ current, red - resonant inductor current i_{Lr} , yellow - magnetizing inductor current i_{Lm}

temperature and circuit parameters and is a good indicator for the value of the minimum required dead time for the selected IGCT switch. Simulation and experimental data is used to measure and discuss t_{DOFF} dependencies in [14].

Maximum limit for the dead-time requirement comes from the LLC-SRC operation. Fig. 2 shows the typical voltage and current waveforms of the anti-parallel IGCT-diode pair in LLC-SRC with positive current conducted by the IGCT while the negative current is supported by the diode. At the moment when the top IGCT, $IGCTD_1$, is turned off, current commutates to the bottom diode and continues to flow through it (small negative $IGCTD_2$ current in Fig. 2) until it reaches zero. Bottom IGCT, $IGCTD_2$, can safely be turned on after the time needed for the top IGCT, $IGCTD_1$, to enter blocking state and this should happen before the bottom diode current falls to zero if the zero voltage turn-on of the $IGCTD_2$ (and vice versa) is to be achieved (case considered in this paper). Non zero voltage turn-on would happen if the current cannot be supported by the $IGCTD_2$ and starts flowing through the top diode of $IGCTD_1$, behavior that would cause increased turn-on losses.

Time needed for the bottom diode current to fall to zero is denoted as t_{DCND} and should be greater than the specified dead time in the system. Mathematically, the dead time requirement for the zero voltage turn-on can be expressed as:

$$t_{DOFF} < t_D < t_{DCND} \quad (1)$$

Turn-off delay time is mainly influenced by the IGCT turn-off current and temperature for the given DC-link voltage and its values can be experimentally obtained or provided by the semiconductor manufacturer. Analysis of the electrical circuit yields a mathematical expression for the switch (IGCT and the anti-parallel diode) current which can be used to calculate the diode conduction time t_{DCND} , having in mind that the negative value represents



Figure 3: Multifunctional laboratory test setup

the current flowing through the diode:

$$i_S(t) = I_{rm} \sin(\omega_r t) + 4I_{off} f_{sw} t - I_{off} \quad (2)$$

under the condition that:

$$i_S(t_{DCND}) = 0 \quad (3)$$

Analytical solution for t_{DCND} under the first order approximation is presented here (Eq. 4) but numerical methods or higher order approximations can be used for improved calculation accuracy.

$$t_{DCND} = \frac{I_{off}}{4I_{off}f_{sw} + 2\pi I_{rm}f_r} \quad (4)$$

Table I: Continuous resonant operation test parameters for different experiments

Parameter	Experiment 1	Experiment 2	Experiment 3
$IGCT_1, IGCT_2$	5SHX 1445H		
D_1, D_2	5SDF 10H4503		
$V_{DC}[V]$	2x1250	2x1250	2x1250
$C_{DC}[\mu F]$	2.6	2.6	2.6
$C_R[\mu F]$	660	660	660
$L_R[\mu H]$	15	15	7.5
$f_R[Hz]$	1600	1600	2260
$f_{SW}[Hz]$	1440	1440	1860
$L_M[mH]$	3	1.5	1.5
$I_{off}[A]$	70	140	100
$I_{rm}[A]$	910	910	910
$t_{DOFF}[\mu s]$	3.4	2.9	3.1
$t_{DCND}[\mu s]$	7.6	14.5	8.1
$t_D[\mu s]$	8	15	8

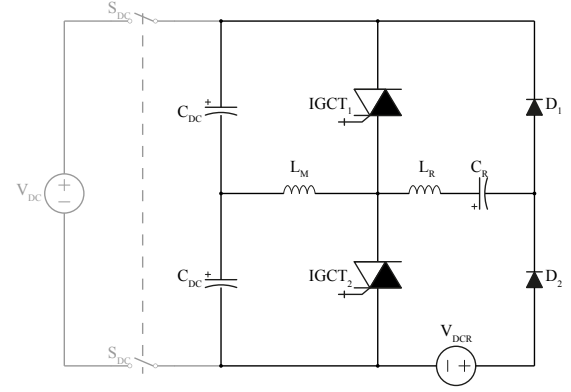


Figure 4: Resonant operation connection diagram of the test setup

III. CHARACTERIZATION TEST SETUP

Test setup, designed and built for gathering experimental data and verification of the theoretical assumptions, is shown in Fig. 3. Connection diagram for testing of the resonant operation of the IGCT in given in Fig. 4. The test setup is employed in double pulse testing [14], resonant pulse testing [15] as well as in testing for the continuous operation under resonant switching. It is shown in [14] and [15] that the regular double pulse test can be used for evaluation of the low current turn-off delay times and the accompanying energy losses. Results are presented in Fig. 5 and Fig. 6 respectively and are used for definition of minimum allowed dead-time, t_{DOFF} from Eq. 1. Resonant tank of the test setup can be tuned for different frequencies for the particular experiment of interest by discretely changing the values for L_R and C_R . Switching frequency of the IGCT half-bridge is commanded by the industrial controller, together with the precalculated dead times.

The upper dead time limit is calculated from Eq. 4 and the predefined design requirements for the IGCT turn-off current and the maximum resonant current. Table I summarizes the setup configuration for each particular test, as well as the required limits for the dead-time selection. Values for the t_{DOFF} are read directly from the graph given in Fig. 5 and diode conduction times are calculated according to Eq. 4. Given that Eq. 4 underestimates the diode conduction times, the dead-times were rounded to the nearest integer of micro-seconds which didn't have any impact on the final operation. Since the t_{DOFF} from Fig.

Table II: Semiconductor switch parameters

	IGCT	Reverse Diode
Manufacturer	ABB	ABB
Model	5SHX 1445H	5SHX 1445H
Forward blocking voltage	5500V	5500V
V_{DC}	3300V	-
I_{TGQM}	900A	-
I_{FVM}	-	170A
Threshold Voltage V_{T0}, V_{F0}	1.65V	2.53V
Slope Resistance r_T, r_F	2mΩ	4.3mΩ

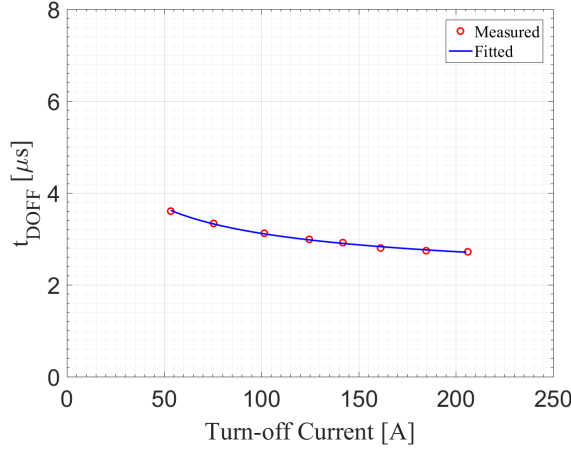


Figure 5: Estimated t_{DOFF} from the experiment, given in [14]

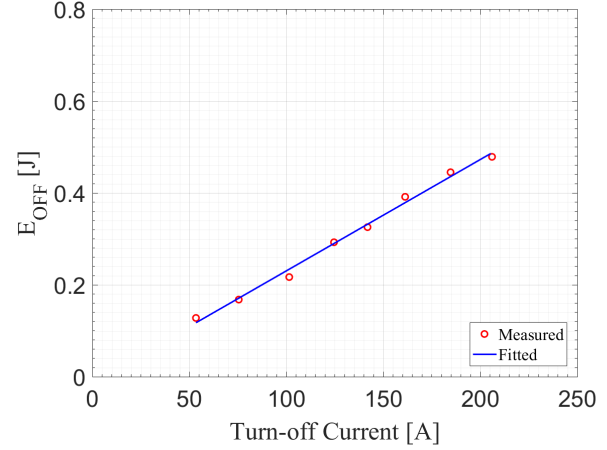


Figure 6: Estimated E_{OFF} from the experiment, given in [14]

5 has been measured for the temperature of 30°C, dead times were chosen to be higher than the two times 30°C values given in the Table I, to account for the t_{DOFF} prolongation with temperature, as presented in [14].

Maximum resonant current for the continuous test is chosen to match maximum turn-off current of the given IGCT ($I_{TGQM} = 900A$) for safety reasons; this value corresponds to the nominal operating power of the LLC-SRC of 670kW. Relevant semiconductor data for the devices used in the test setup is given in Table II.

Conduction power losses P_{CND} and respective switching power losses P_{SW} are presented in the Table III. Calculations and estimations are done using the following equations:

$$P_{CND} = V_{T0}I_T^{avg} + r_T(I_T^{rms})^2 \quad (5)$$

$$P_{SW} = E_{OFF}f_{SW} \quad (6)$$

where I_T^{avg} and I_T^{rms} are average and root-mean-square values of the IGCT current respectively, V_{T0} is a threshold voltage and r_T is the slope resistance. E_{OFF} is the turn-off energy of the IGCT given for the specific turn-off current and f_{SW} is the switching frequency. Conduction losses of the free-wheeling diode are estimated as well, while the losses due to reverse recovery are neglected; this is justified since the diode's di/dt during the turn-off is very low in this application. As the calculation showed the numbers within the datasheet limits of the semiconductor devices, experiments were run to confirm the predicted operation of the test setup.

IV. EXPERIMENTAL RESULTS

Experiments were run as defined in Table I and all the experiments were executed successfully meaning that the results were collected for the further analysis and there were no major issues during the switching of the IGCT half-bridge. Typical waveforms of the currents and voltages for the $IGCT_1$ and the $IGCT_2$ are presented in Fig. 7 for the two distinct switching frequencies: 1440Hz and 1860Hz.

It is noticed immediately that the currents are not symmetrical and that there is a slight deviation in the resonant current half-period between $IGCT_1$ and $IGCT_2$. Referring to Fig. 4, a voltage source V_{DCR} can be seen in the bottom branch. This is a low voltage, high current source, responsible for maintaining the resonance in the $L_R - C_R$ branch, which would otherwise decrease to zero over time due to the thermal losses in the cables and passive components. V_{DCR} is connected between the cathode of $IGCT_2$ and the anode of D_2 using a relatively long, high-current cables, extending outside of the test setup cabinet. The similar connection is made between the cathode of D_1 and anode of $IGCT_1$ but using much shorter cable. The difference in the parasitic inductance between these two connections causes slightly different resonant circuit parameters i.e. parasitic inductance of the conducting branch adds to the resonant inductance L_R , changing the resonant frequency and maximum of the resonant current for the two IGCTs. As the source of unbalance can be clearly identified, no care is taken to add extra cables and match resonant circuit during positive and negative half-cycles.

The turn-off current of the IGCT is kept constant

Table III: Estimation of the conduction and switching losses for the switching half-bridge

Parameter	Experiment 1	Experiment 2	Experiment 3
$I_T^{avg}[A]$	261	262	240
$I_T^{rms}[A]$	428	427	403
$P_{CND}^T[W]$	797	797	721
$E_{OFF}^T[J]$	0.16	0.33	0.23
$P_{SW}^T[W]$	230	475	428
$I_D^{avg}[A]$	0.4	1.5	0.8
$I_D^{rms}[A]$	4.4	12	8.0
$P_{CND}^D[W]$	1.0	4.4	2.3
$P_{TOTAL}[kW]$	2.1	2.6	2.3

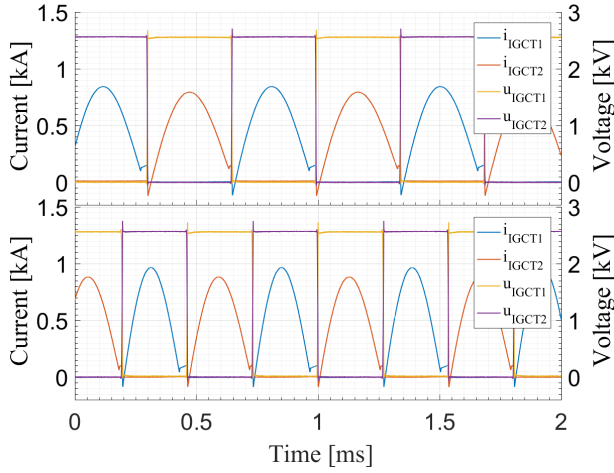


Figure 7: Experimental waveforms (voltage and current) for the continuous operation of the $IGCT_1$ and $IGCT_2$ under the resonant operating conditions: top $f_{SW} = 1440Hz$, bottom $f_{SW} = 1860Hz$

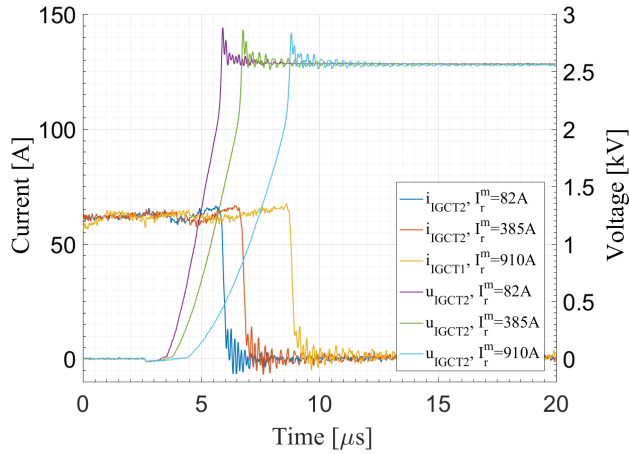


Figure 8: Turn-off waveforms current and voltage $f_{SW} = 1440Hz$, $I_{OFF} = 70A$

between the two switches and behaving as expected. It should be noted that the IGCT half-bridge works without any clamp circuit. Hard-switching applications of the IGCT require a clamping circuit mainly to protect the free-wheeling diodes from the excessive di/dt during the turn-on of the IGCT. In case of LLC-SRC operation, diode's turn-off di/dt is limited by the resonant tank and its value is much lower than what is found in the hard-switching application. This makes the clamping circuit redundant and it is left out of the design with no penalty regarding the diode turn-off behavior. Removal of the clamp circuit positively impacts the overall power density of future IGCT-based DC-DC converter designs.

One possible drawback of the missing clamp circuit is that the short circuit current of the half-bridge is not limited by the clamping inductor anymore but only by the bus-bar's parasitic inductance and can reach much higher values than those found in the hard-switching applications. Different means of protection of the DC-link

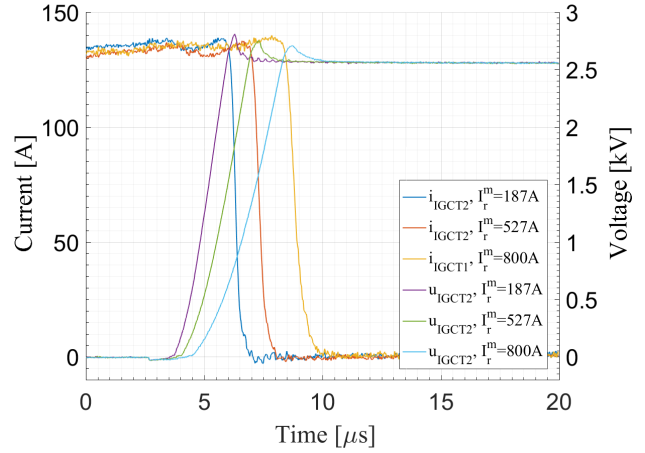


Figure 9: Turn-off waveforms current and voltage $f_{SW} = 1440Hz$, $I_{OFF} = 140A$

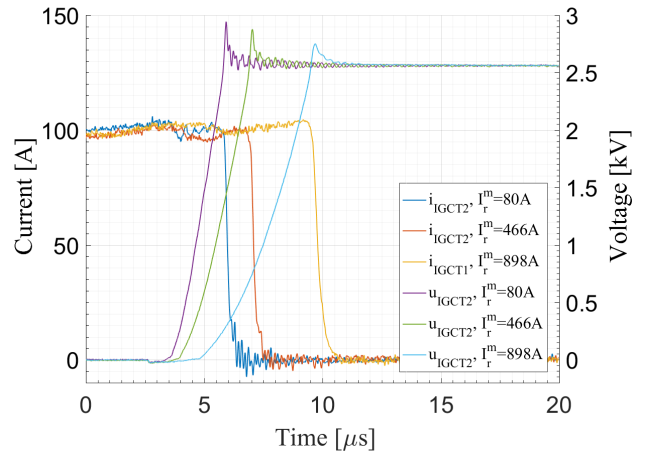


Figure 10: Turn-off waveforms current and voltage $f_{SW} = 1860Hz$, $I_{OFF} = 100A$

and the switching elements should be employed but this is out of the scope of the paper.

Fig. 8, 9 and 10 show the turn-off periods for the three different experiments performed on the test setup. Fig. 8 shows the current and voltage waveforms of the $IGCT_2$ during the continuous operation with $f_{SW} = 1440Hz$, turn-off current of 70A and three different resonant (load) currents: 82A, 385A and 910A. Fig. 9 and 10 show the same turn-off periods but for the working switching frequencies of 1440Hz and 1860Hz respectively.

All the waveforms are synchronized with the optical signal, controlling the gate driver, going low i.e. turn-off command. Zero point on the time axis represents this moment but the turn-off signal itself is not shown for the clarity purposes.

First thing that can be noticed in the waveforms is that the turn-off delay time, t_{DOFF} varies with the load current. The t_{DOFF} parameter is summarized with the plot in Fig. 11 with values measured from all of the waveforms from the three experiments. This finding could lead to a conclusion that the t_{DOFF} is a function of the

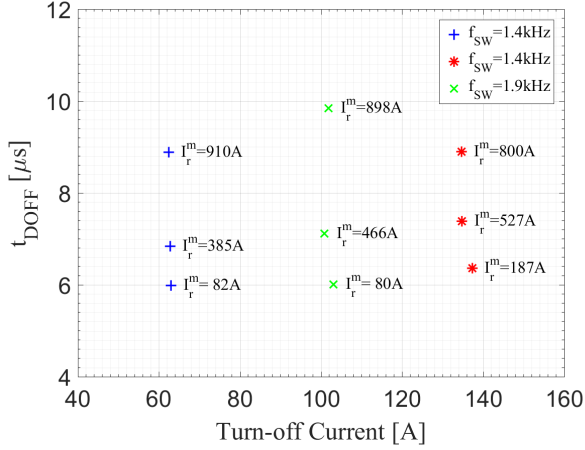


Figure 11: Turn-off delay time estimated from the experimental current and voltage waveforms

maximum resonant (load) current through the device but there is a lurking variable present here: the IGCT junction temperature. It must be noted that the temperature of the junction was not controlled and kept constant during the experiments; cooling inlet water temperature was kept at the 30°C, as this was the only controllable temperature in the system. It was shown in the previous work [15], through simulation and experiment, that t_{DOFF} mostly depends on the junction temperature and the value of the turn-off current of the IGCT when the blocking voltage is kept constant (2.5kV in this case). This is also made evident by comparing results in Fig. 5 and Fig. 11.

As the power losses of the IGCT vary considerably with the maximum of the load (resonant) current, the prolongation of the t_{DOFF} is accounted to the change in temperature of the semiconductor junction. With a test setup running in a continuous regime and relatively low thermal junction-to-heatsink constant of the IGCT, the waveform triplets represent the samples at a working temperature corresponding to the given load at the moment of the recording of the waveforms. The higher the load current, the higher the working temperature of the IGCT that influences the t_{DOFF} parameter by prolonging it.

The same explanation holds the turn-off energy losses depicted in the Fig. 12, estimated by the time integration of the product of the IGCT's current and voltage waveforms during the turn-off period. The delays originating from the current and voltage measurement methods (probe delays, cable propagation delays) were already accounted for by setting the respective deskew delays on the measuring channels of the oscilloscope. Proper aligning of the current and voltage waveforms is essential for this method of the turn-off losses evaluation.

Comparing the results in Fig. 6 and Fig. 12, it can be seen that the turn-off energy losses are higher in the later figure. This result is expected simply because the Fig. 6 summarizes the double pulse test results at the junction temperature of 30°C while Fig. 12 shows the results under the continuous load conditions directly influencing the

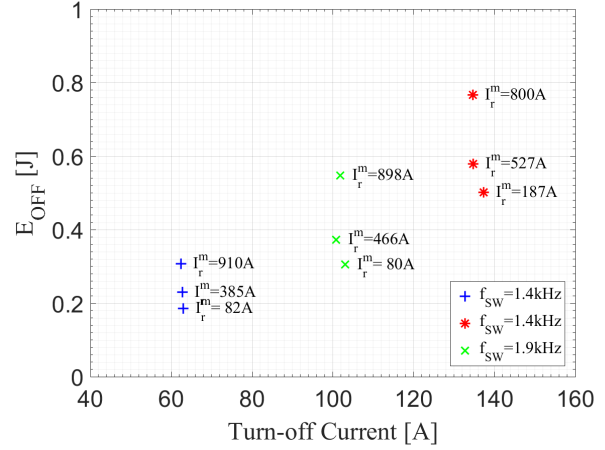


Figure 12: Estimated turn-off energy losses

junction temperature of the IGCT.

By comparing the values in Fig. 12 and the estimations done before running the experiments from Table III, it can be noted that the IGCT switching losses become a considerable portion of the total losses of LLC-SRC half bridge. In order to have even higher switching frequencies of the converter, switching losses have to be lowered, either by lowering the turn-off current or by choosing an IGCT device optimized for switching rather than conduction losses. Allowing for the higher temperature rise of the semiconductor by lowering the thermal conductivity of the case is another solution but this one comes at the cost of lower efficiency of the converter.

One more issue that can be noted in the turn-off waveforms in Fig. 8 and Fig. 10 is rather oscillatory turn-off of the IGCT. The response can be improved by lowering the parasitic inductance of the DC-link bus-bars connecting the half-bridge and the DC-link in order to provide better attenuation of the system. If the decrease of the parasitic inductance of this commutation loop is not possible, the turn-off current of the IGCT has to be increased to counteract the ringing, since these oscillations could cause the electromagnetic interference problems and the additional losses.

V. CONCLUSION

This paper shows the challenges that must be overcome for application of the IGCT semiconductor switch in LLC-SRC. Theoretical considerations show what compromises have to be made between high frequency operation of the converter and switching energy losses and how the design parameters such as maximum resonant current, turn-off delay time and IGCT turn-off current influence the choice of dead-time in the system and maximum possible safe switching frequency.

The experiment has shown a successful application of the IGCT in the test setup providing LLC-SRC current/voltage stress environment for the semiconductor switch. Safe operation of the half-bridge was demonstrated under relatively high switching frequency for this kind of

a high voltage switch, typically employed in the hard-switching applications with up to 900Hz switching frequency. Exclusion of the clamp circuit was proven justified and the clamp-less operation of the IGCT was achieved and demonstrated.

Turn-off delay time parameter evaluation and turn-off losses estimation using a double-pulse data proved to be useful in the first step during the design process of the converter. High temperature double-pulse data would be more helpful for the final design and will be considered for the future works by the authors. Measuring the parameters on the test setup working in continuous mode of operation gave the further insight into temperature influence of the turn-off behavior and the lessons learned pave way for reaching even higher operation frequencies.

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